Remarks

Claims 22-39 are presently active, claims 1-21 having been cancelled without prejudice by this Amendment and new claims 22-39 added by this Amendment.

In the office action dated 5 December 2001 ("Office Action"), the title of the invention was objected to as not being descriptive; claims 1-21 were rejected under 35 U.S.C. §102(b) as being anticipated by Sundstrom, U.S. patent 5,602,494 ("Sundstrom"); claims 1-3, 5-12, and 14-18 were rejected under 35 U.S.C. §102(b) as being anticipated by Cooperman et al., U.S. patent 5,045,730, ("Cooperman"); and claims 4 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Cooperman in view of Yokota et al., U.S. patent 5,635,859 ("Yokota").

The title is amended to be more descriptive of the invention.

To better define and more particularly point out the present invention, claims 1-21 are cancelled without prejudice, and new claims 22-39 are added. Applicants believe that all presently active claims are neither anticipated nor obvious in view of the references of record. Because Yokota was cited in the Office Action merely for teaching that a resistor may be replaced by a field effect transistor, the argument below regarding patentability need only be directed to Sundstrom and Cooperman.

All presently active claims include a transmission line having a quiescent voltage at the ground voltage of the electronic system. Sundstrom and Cooperman do not teach a transmission line having the ground voltage as its quiescent voltage. Referring to Fig. 1 of Sundstrom, the combination of resistors 131 and 132 forms a voltage divider to provide a bias voltage at external interconnect 190, so that the quiescent voltage of the external interconnect is not at ground voltage. Referring to Fig. 4 of Cooperman, the resistor network R7 and R8 biases to a voltage other than ground voltage, and consequently the transmission line as taught in Cooperman does not have a quiescent voltage at ground voltage. Consequently, all presently active claims are distinguishable over the cited references of record.

Furthermore, some of the claims are further distinguishable over Cooperman because Cooperman does not teach that the sources of the pMOSFETs are biased to a core voltage. Referring to Fig. 4 of Cooperman, a CMOS interface circuit comprising

circuitry 30 allows a ECL circuit (agent) connected to 31 at the left of Fig. 4 to communicate with a CMOS circuit (agent) connected to 33 at the right of Fig. 4. See for example the bottom of column 2 to the top of column 3, which although is in reference to Fig. 2, nevertheless applies also to Fig. 4 because Fig. 4 is simply a Thevenin equivalent to Fig. 2. (See the last paragraph in column 3 regarding the Thevenin equivalent.) Note that the pullup pMOSFETs in CMOS interface circuit 30 have their sources at a voltage V_{DD}. The voltage V_{DD} is not the core voltage of the ECL agent and it is not the core voltage of the CMOS agent. As taught in column 3, second paragraph, V_{DD} is chosen at 1.3 volts to shift the input threshold voltage for the CMOS interface circuitry 30 to -1.2 volts. Note that the logic levels for ECL logic as taught in column 1, second paragraph, are -1.6 volts and -0.8 volts, and the logic levels for CMOS logic are 0 volts and 5 volts.

Claims 22-34 include a pMOSFET (to drive the transmission line) having a source at the core voltage, and are thus further distinguishable over Cooperman. Sundstrom is silent as to whether the sources of its disclosed pMOSFETs are at the core voltage of the die, but Sundstrom does not teach this limitation, so it may be argued that claims 22-34 are further distinguishable over Sundstrom as well.

Claims 23-28 also include first and second pMOSFET having sources at a first and second core voltage, respectively. None of the cited references of record teach this, and thus these claims are further distinguishable over the cited references of record.

Claims 26, 28, 30, and 35-37 include an agent connected to a transmission line other than at one of the ends of the transmission line. None of the cited references of record teach this, and thus these claims are further distinguishable over the cited references of record.

An Information Disclosure Statement citing three references from an international search report is filed herewith. In particular, applicants wish to bring to the Examiner's attention U.S. patent no. 5,638,402 (e.g., see Figs. 1 and 6), included with the IDS.

Respectfully submitted,

Seth Z Kalson Dated: June 4, 2002

Seth Z. Kalson
Reg. no. 40,670
Attorney for Applicants and Intel Corporation (Assignee)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D C. 20231

on 10/4/02
Date of Deposit

Dana Roberts
Name of Person Mailing Correspondence

Signature 10/4/02
Date

Version of Amended Specification with Changes

The title on page 1 is amended as follows:

Input-Output Bus Interface <u>to Bridge Different Process Technologies</u>